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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,529	02/17/2004	Jong-Rong Jan	9180-30	1502

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EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/780,529	JAN ET AL.
	Examiner	Art Unit
	Chuong A. Luu	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 36-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 36-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/04;2/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of Group I, claims 1-23 and 36-48 in the reply filed on June 30, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1-23 and 36-48 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashimoto (U.S. 6,475,896 B1).

Hashimoto discloses a semiconductor device with

(1); (48) forming a barrier layer (20) on the substrate (10) including the metal layer (16);

forming a conductive bump (26) on the barrier layer (20) wherein the barrier layer (20) is between the conductive bump (26) and the substrate (10) and wherein the conductive bump (26) is offset from the metal layer (16) (see Figure 3A-3D);

after forming the conductive bump (26), removing at least some of the barrier layer (20) from the metal layer (16) thereby exposing the metal layer (16) while maintaining a portion of the barrier layer (20) between the conductive bump (26) and the substrate (10) (see Figure 3A-3D);

(2) wherein the substrate comprises an integrated circuit substrate (see Figure 3A-3D);

(3) wherein the metal layer comprises an alluminum layer;

(4) wherein the barrier layer comprises a layer of TiW;

(5) wherein the metal layer, the barrier layer, and the conductive bump all comprise different materials (see Figure 3A-3D);

(6) further comprising: before forming the conductive bump, forming a conductive under bump metallurgy layer on the barrier layer; and before removing the barrier layer, removing the conductive under bump metallurgy layer from the barrier layer opposite the metal layer while maintaining a portion of the conductive under bump metallurgy layer between the conductive bump and the substrate (see Figure 3A-3D);

(7) wherein the conductive under bump metallurgy layer comprises copper (see column 11, lines 1-30);

(8) wherein the conductive under bump metallurgy layer and the barrier layer comprise different materials (see Figure 3A-3D);

(9) further comprising: before forming the conductive bump, forming a second barrier layer on the under bump metallurgy layer wherein the second barrier layer and the under bump metallurgy layer comprise different materials and wherein the second barrier layer is between the conductive bump and the conductive under bump metallurgy layer (see Figure 3A-3D);

(10) wherein the second barrier layer comprises nickel;

(11) wherein the under bump metallurgy layer comprises copper;

(12) wherein forming the second barrier layer comprises selectively forming the second barrier layer on a portion of the under bump metallurgy layer wherein the second barrier layer is offset from the metal layer (see Figure 3A-3D);

(13) wherein forming the conductive bump comprises selectively forming the conductive bump on the second barrier layer offset from the metal layer (see Figure 3A-3D);

(14) wherein selectively forming the second barrier layer and selectively forming the conductive bump comprise selectively forming the second barrier layer and the conductive bump using a same mask (see Figure 3A-3D);

(15) wherein the conductive bump comprises at least one of solder, gold, and/or copper;

(16) wherein forming the conductive bump comprises selectively plating the bump on the barrier layer offset from the metal layer (see Figure 3A-3D);

(17) wherein the integrated circuit substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the

input/output pad, and wherein the conductive bump is formed on the barrier layer opposite the input/output pad (see Figure 3A-3D);

(18) wherein the metal layer and the bump pad both comprise aluminum;

(19) wherein the substrate includes an input/output pad thereon, wherein the barrier layer is formed on the substrate including the metal layer and the input/output pad, and wherein after removing the barrier layer from the metal layer, the conductive bump is electrically coupled to the input/output pad (see Figure 3A-3D);

(20) wherein the metal layer and the input/output pad both comprise aluminum;

(21) wherein the conductive bump is formed on the barrier layer opposite the input/output pad (see Figure 3A-3D);

(22) wherein the conductive bump is offset from the input/output pad (see Figure 3A-3D);

(23) further comprising: after removing the barrier layer from the metal layer, bonding a second substrate to the conductive bump (see Figure 3A-3D);

(36) forming a barrier layer on the substrate offset from the exposed metal layer;

forming a conductive bump on the barrier layer wherein the barrier layer is between the conductive bump and the substrate, wherein the conductive bump is offset from the metal layer, and wherein the barrier layer, the conductive bump, and the metal layer all comprise different conductive materials (see Figure 3A-3D);

(37) wherein the electronic device comprises an integrated circuit device, and wherein the substrate comprises an integrated circuit substrate (see Figure 3A-3D);

(38) wherein the barrier layer comprises titanium tungsten;

(39) wherein the exposed metal layer comprises aluminum;

(40) wherein the conductive bump comprises at least one of solder, gold, and/or copper;

(41) further comprising: forming a conductive under bump metallurgy layer between the barrier layer and the conductive bump (see Figure 3A-3D);

(42) further comprising: bonding a second substrate bonded to the conductive bump (see Figure 3A-3D);

(43) wherein the integrated circuit substrate includes an input/output pad thereon and wherein the barrier layer and the conductive bump are electrically connected to the input/output pad (see Figure 3A-3D);

(44) wherein the input/output pad and the metal layer each comprise aluminum (see Figure 3A-3D);

(45) wherein the conductive bump is on the barrier layer opposite the input/output pad (see Figure 3A-3D);

(46) wherein the conductive bump is offset from the input/output pad (see Figure 3A-3D);

(47) further comprising: an under bump metallurgy layer between the barrier layer and the conductive bump wherein the under bump metallurgy layer and the barrier layer comprise different materials (see Figure 3A-3D).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
July 25, 2005